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(54) INTEGRATED ATM/PACKET SEGMENTATION-AND-REASSEMBLY ENGINE FOR HANDLING BOTH PACKET AND ATM INPUT DATA AND FOR OUTPUTTING BOTH ATM AND PACKET DATA

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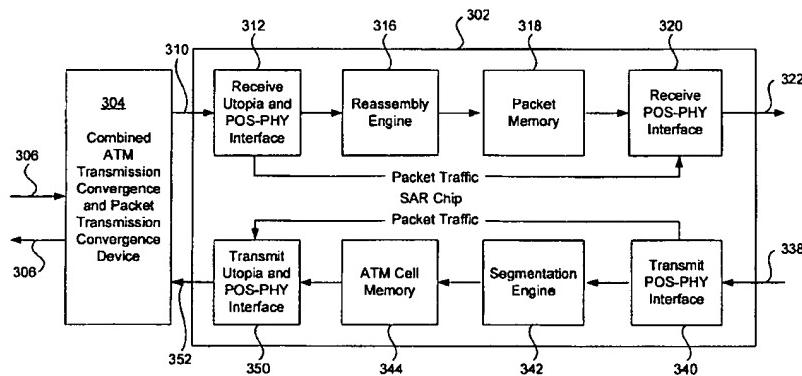
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Assistant Examiner—Christopher M Swickhamer

(57) ABSTRACT

An integrated ATM/packet segmentation-and-reassembly engine for handling both packet and ATM input data and outputting packets containing information from both the packet and ATM input data. The integrated ATM/packet segmentation-and-reassembly engine is also configured for receiving packets containing information destined for transmission as ATM cells and information destined for transmission as packets, perform the segregation function and segmentation function on the information destined for transmission as ATM cells in order to output both ATM cells and packets. Architecture includes the ability to output both ATM cells and packets on a single optical fiber.

19 Claims, 9 Drawing Sheets

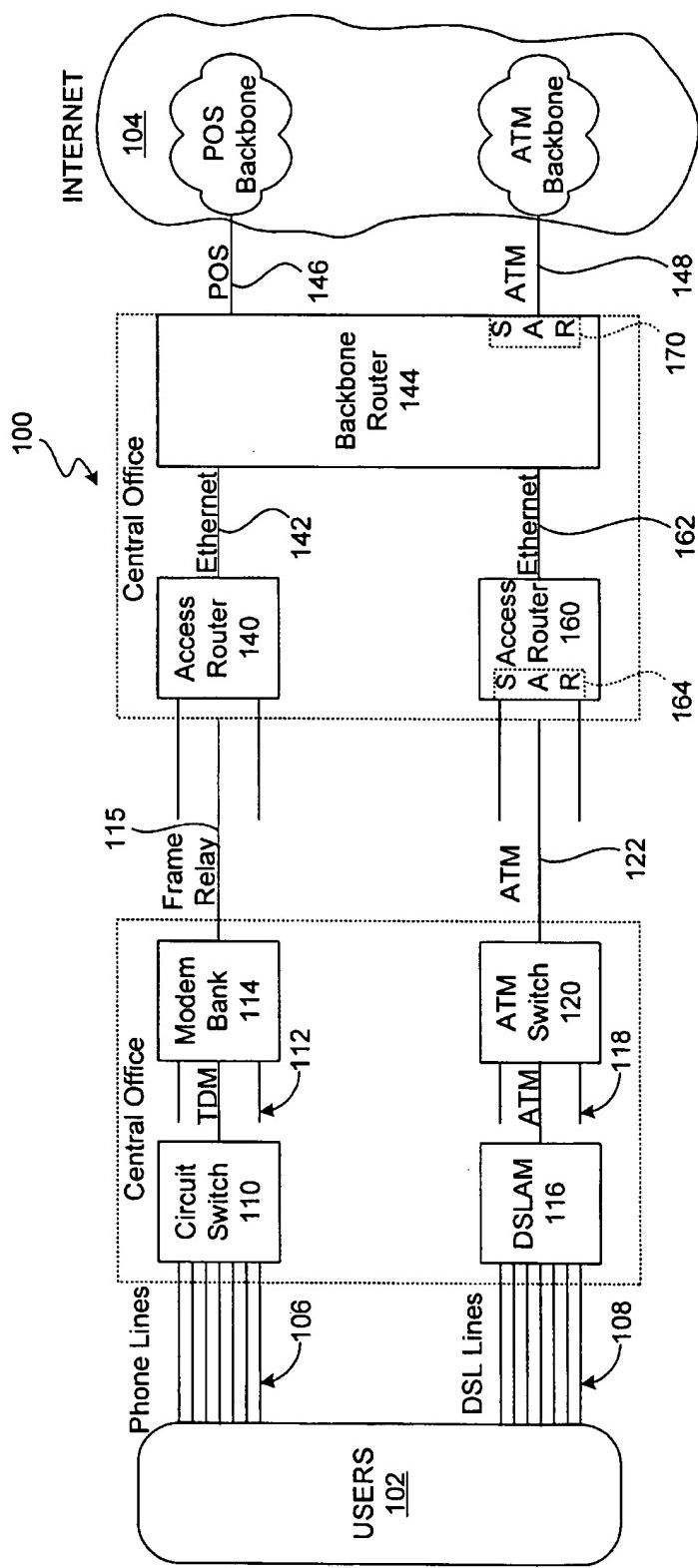


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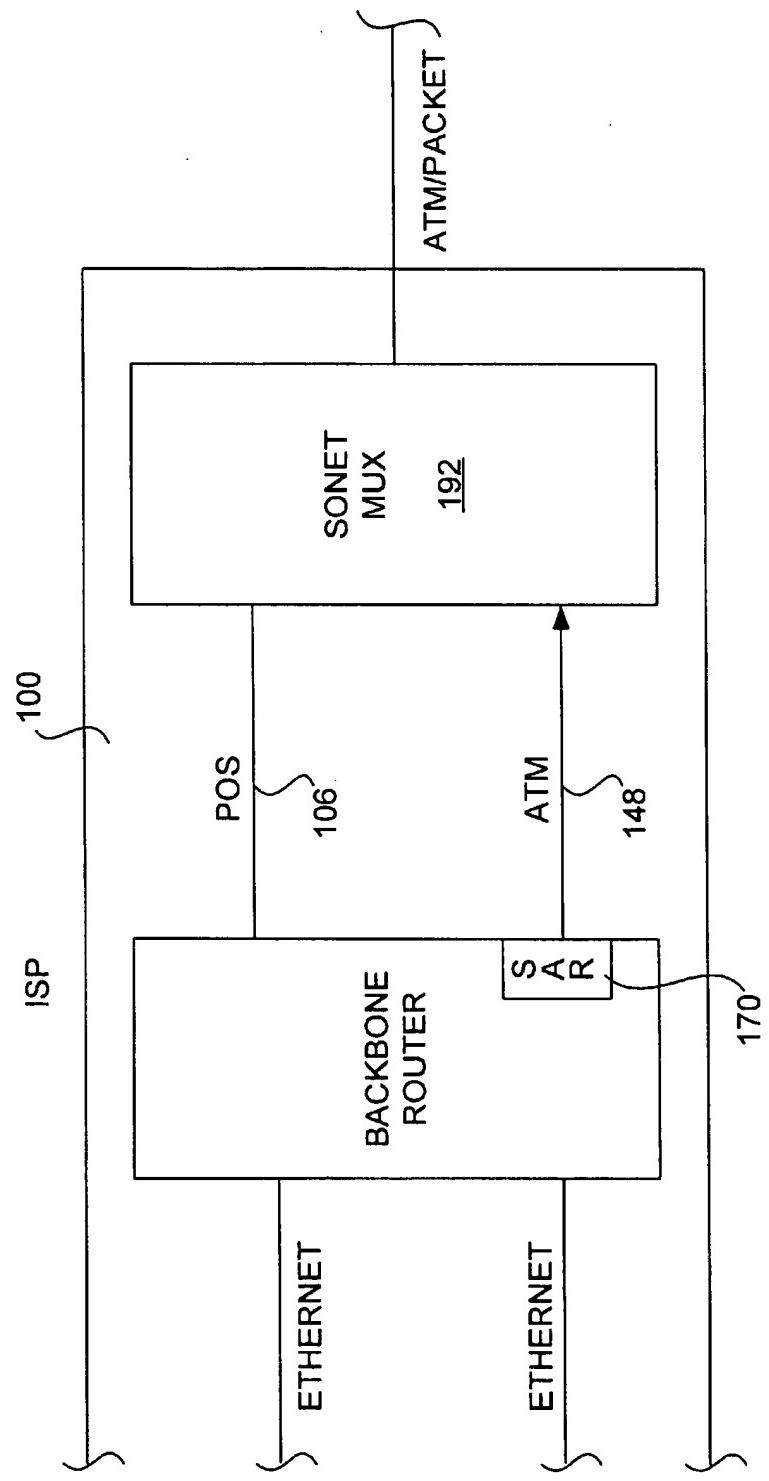
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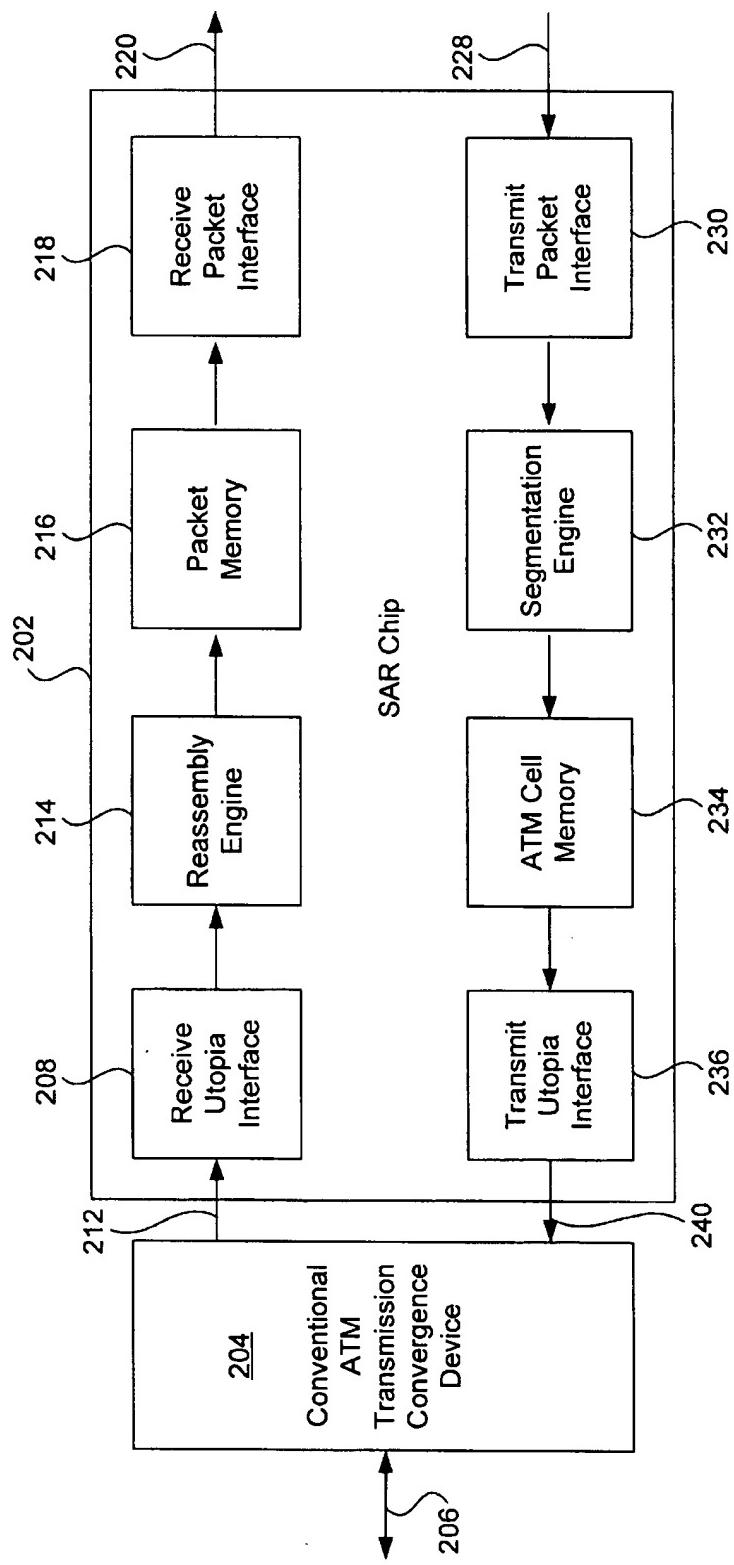
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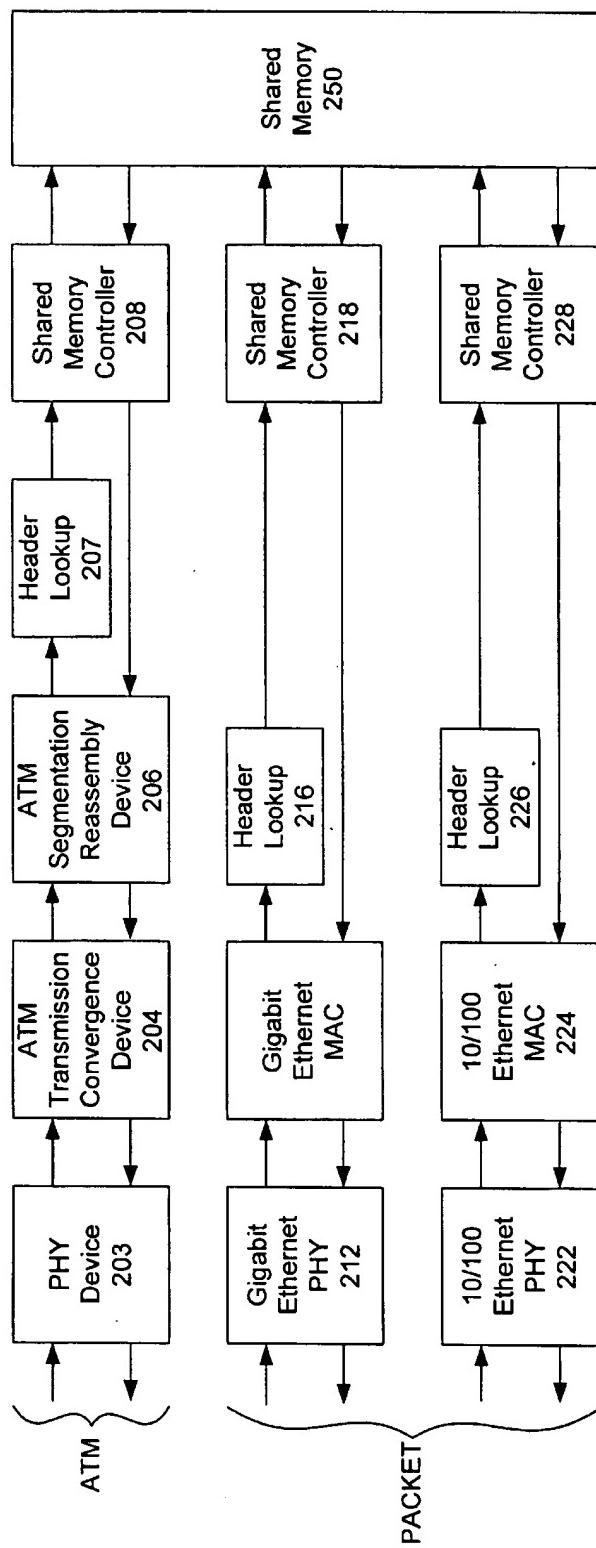
**FIG. 1A
(PRIOR ART)**



**FIG. 1B
(PRIOR ART)**



**FIG. 2A
(PRIOR ART)**



**FIG. 2B
(PRIOR ART)**

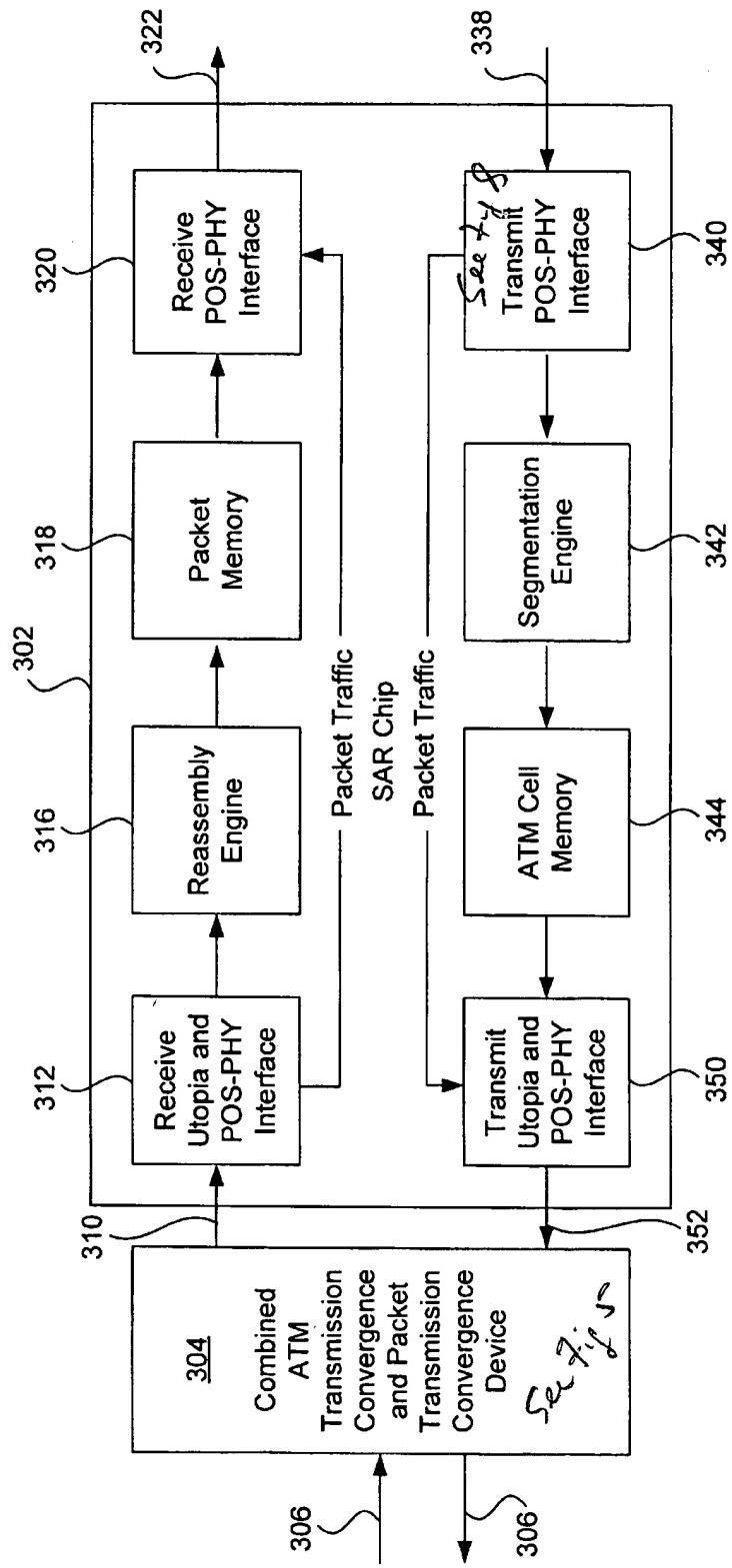


FIG. 3

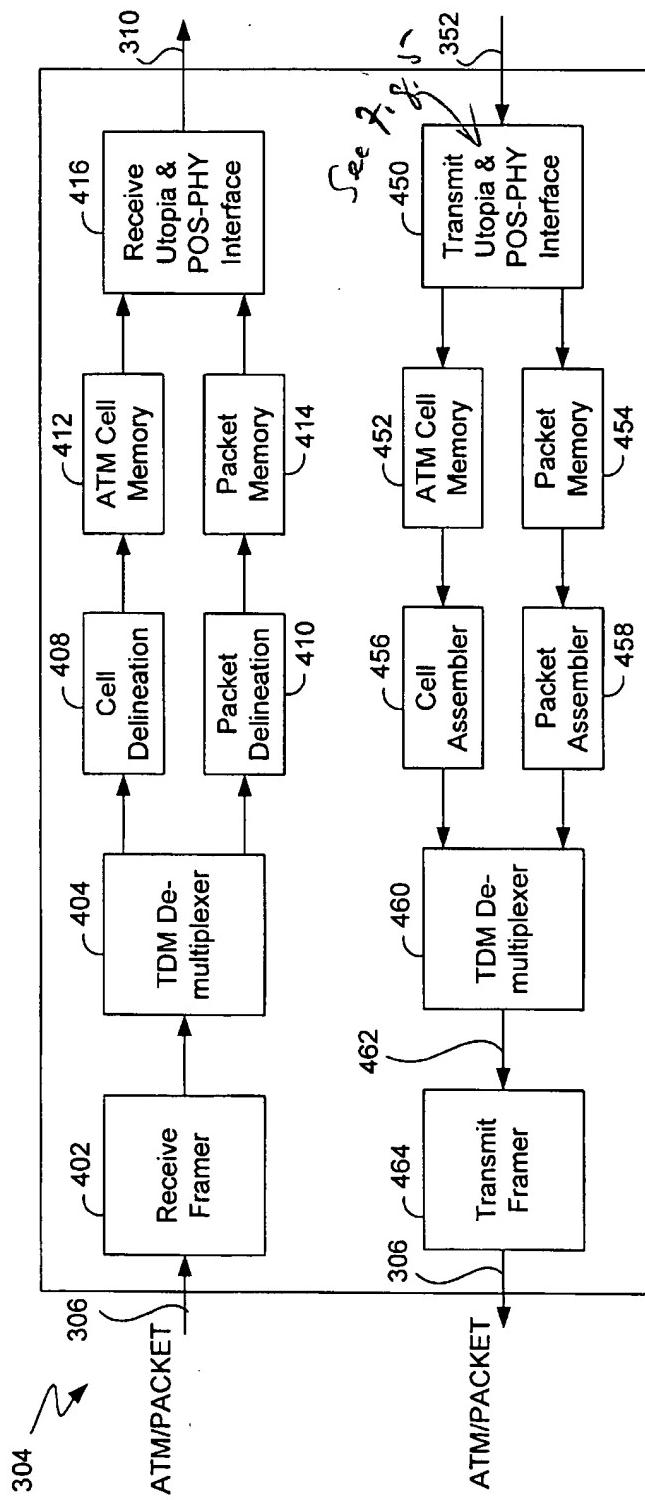


FIG. 4

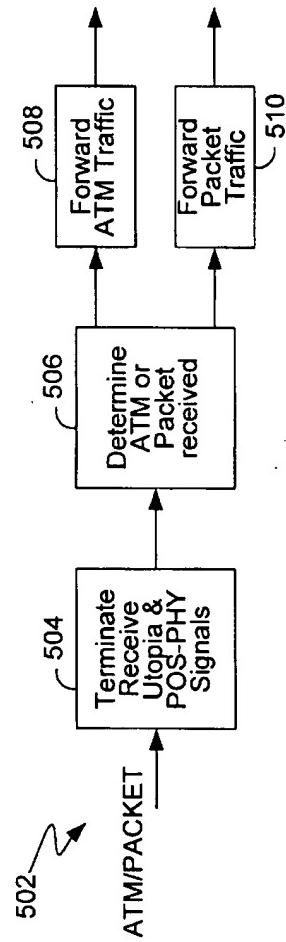


FIG. 5

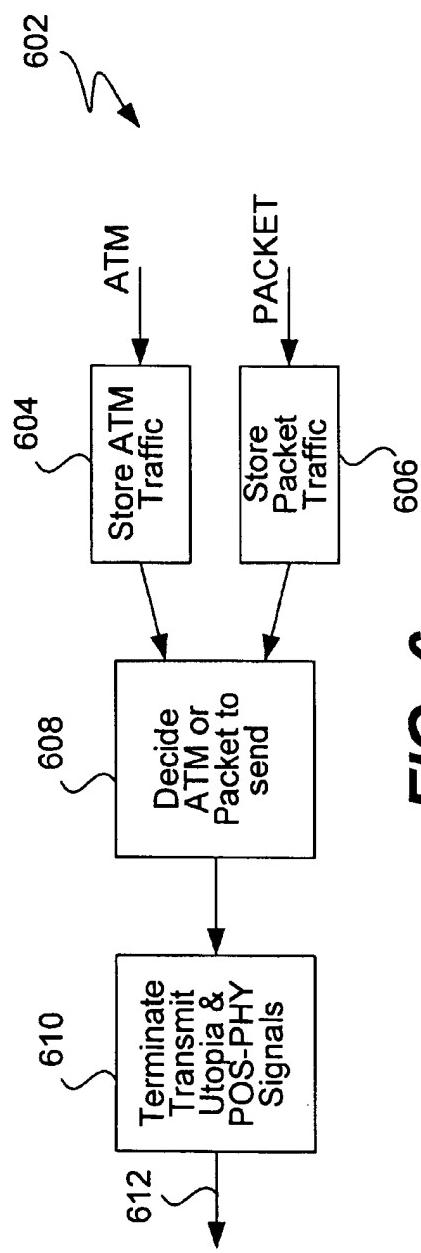


FIG. 6

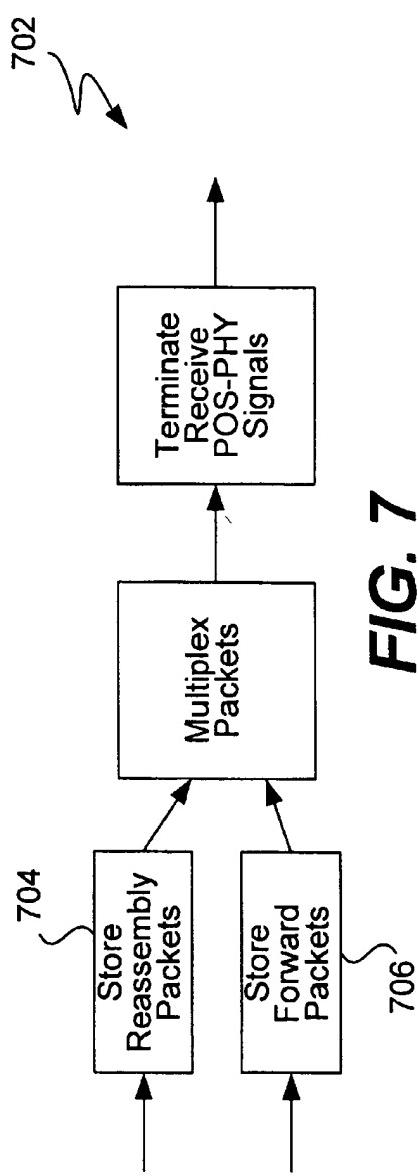


FIG. 7

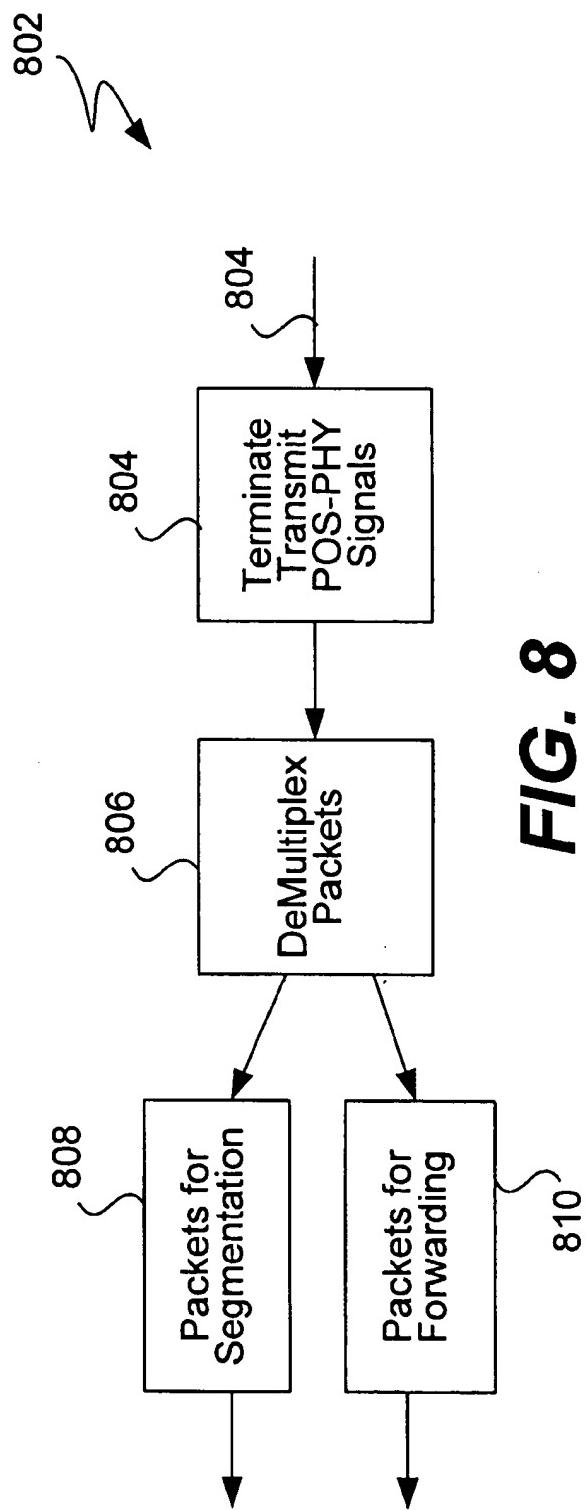


FIG. 8

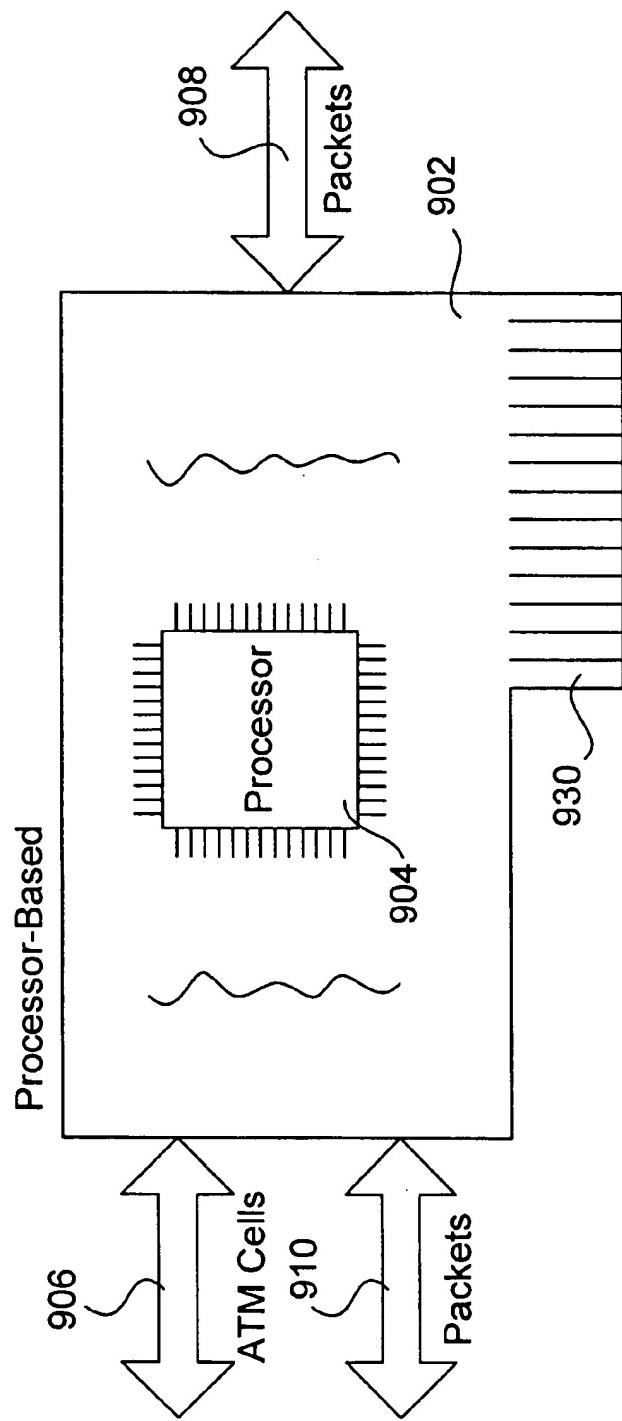


FIG. 9

**INTEGRATED ATM/PACKET
SEGMENTATION-AND-REASSEMBLY
ENGINE FOR HANDLING BOTH PACKET
AND ATM INPUT DATA AND FOR
OUTPUTTING BOTH ATM AND PACKET
DATA**

BACKGROUND OF THE INVENTION

The present invention relates to improved techniques for facilitating the transmission of data among disparate communication networks. More particularly, the present invention relates to improved devices and methods for facilitating transmission of packet data traffic and ATM data traffic on a single communication link.

With the information revolution and particularly with the rise of the Internet and the voice/data/video convergence, the volume of data to be sent and received over various communication networks have increased exponentially in recent years. Data, as the term is utilized in the present invention, relates to digital data that may be employed to carry voice, video, or any other information (such as text, graphics, and the like) that can be represented as a digital signal. To cope with the exponential increase in the amount of data being transmitted and received, network technologies have evolved as well. Nowadays, two dominant network technologies have emerged: packet-based technology and asynchronous transfer mode-based (ATM) technology. Packet technology includes TCP/IP, token ring, etc. One example of packet technology is IP (Internet Protocol) packets transmitted over OSI layer 2. Another example of packet technology is Ethernet. ATM technology is well known and well defined and will not be elaborated further here.

For a while, it appears that ATM may be the dominant technology for future communication networks. Accordingly, many businesses spent heavily to convert their existing networks to ATM technology. The emergence of the Internet has caused many to rethink their network strategy, and nowadays, many believe that packet-based technologies represent the wave of the future. Accordingly, some of the earlier adopters of ATM technology, as well as new customers, have chosen packet-based technology as their preferred networking technology. As a result, the customer base currently employs both ATM technologies and packet-based technologies. For data communication among these customers to take place seamlessly, a translation device is required.

In the prior art, one of the devices that translates between ATM data and packet data is generally known as a segmentation-and-reassembly (SAR) engine. The SAR engine typically resides at a location in the network where data from different customers and/or subnetworks is switched. FIG. 1A illustrates an Internet service provider 100, representing one such location in the current network where SAR engines may be found. Referring now to FIG. 1A, a portion of the communication network for allowing Internet users 102 to access the Internet 104 is shown. For the purpose of the present example, Internet users 102 are shown accessing the Internet through either phone lines 106 or DSL (Digital Subscriber Lines) 108, although other access technologies may also be utilized with the present invention.

In the case of phone lines 106, the user typically achieves Internet access through a dial-up connection. Multiple dial-up connections are aggregated at a circuit switch 110, which time-division multiplexes data from a plurality of dial-up

connections into a (TDM) time-division-multiplexed stream to be transmitted via a TDM link 112. The TDM link 112 is terminated at a modem bank 114, which converts the TDM data into packet data for transmission through a wide area network packet link, such as frame relay link 115.

As shown in FIG. 1A, frame relay link 115 terminates at an access router 140, which routes data from multiple frame relay links onto an internal packet link, such as an Ethernet link 142. Ethernet link 142 represents the internal local connection within ISP 100, which interconnects among its server computers (not shown to simplify the illustration). Ethernet link 142 connects with a backbone router 144 as shown, which then routes the data received from the Ethernet link(s) to either a backbone packet link 146 (which may be, for example, packet over SONET or packet over DWDM) or a backbone ATM link 148 for transmission out to Internet 104. One skilled in the art should readily appreciate that the aforementioned steps are reversed when data destined for a user on one of dial-up connections 106 is received at ISP 100 from the Internet 104 through either backbone ATM link 148 or backbone packet link 146.

In the case of DSL lines 108, the individual DSL lines are terminated at a DSL Access Multiplexer 116, which combines the DSL data from a plurality of DSL channels into an ATM stream to be transmitted via an ATM link 118 to an ATM switch 120. ATM switch 120 multiplexes data from various ATM links 118 for transmission via a wide area network ATM link such as ATM link 122. As in the case of frame relay link 115, ATM link 122 also couples to an access router of ISP 100, shown in FIG. 1A as access router 160. However, because the packet-oriented protocol on Ethernet link 162 internal to ISP 100 is different from the ATM protocol on ATM link 122, a translation device is necessary. That translation device is shown in FIG. 1A as the segmentation-and-reassembly (SAR) engine 164. SAR 164 will be discussed in greater detail in FIG. 3 below.

Once the data on ATM link 122 is translated into packet-oriented data and routed to backbone router 144 (via Ethernet link 162 and the server computers of ISP 100), the data is then routed by backbone router 144 to either a backbone packet link 146 or a backbone ATM link 148 for transmission out to Internet 104. In the case wherein data is routed to ATM link 148 from ISP 100, the packet-oriented data is translated via a SAR 170 to ATM cells. One skilled in the art should readily appreciate that the aforementioned steps are reversed when data destined for a user on one of DSL connections 108 is received at ISP 100 from the Internet 104 through either backbone ATM link 148 or backbone packet link 146.

As seen in FIG. 1A, two physical backbone links (comprising at least four separate optical fibers since each optical fiber carries information in only a single direction) are required to allow ISP 100 to handle both ATM traffic and packet-oriented traffic. At the cost of tens of thousands of dollars to purchase and/or lease each optical fiber to implement each backbone link (such as backbone packet link 146 or backbone ATM link 148), this arrangement imposes a high economic burden on ISP operators and other network operators. The high cost for these separate optical links are also hard to justify in view of technologies such as dense wave division multiplex (DWDM), which allows an existing optical fiber to carry much more data per optical fiber than possible previously. Thus, some ISP may find that they still need to bear the economic burden of paying for two fibers in each direction in order to accommodate both ATM traffic and packet-oriented traffic when neither fiber may be employed at anywhere near their full bandwidth capacity.

In the prior art, one of the backbone links may be eliminated through the use of a SONET (synchronous optical network) multiplexer. As shown in FIG. 1B, a SONET multiplexer 192 is located at the Internet-side of ISP 100 and is coupled to both backbone packet link 106 and backbone ATM link 148 on the ISP side. On the Internet-side of SONET multiplexer 192, a single optical channel may be employed to transport both packet-oriented data and ATM data. However, a SONET multiplexer is an expensive and complex electronic system, costing upwards of fifty thousand dollars (\$50,000) or more in some cases and increasing the maintenance burden on the operators. Thus, although the use of a SONET multiplexer theoretically allows ISP operators to avoid paying for separate backbone links to connect to the Internet to accommodate ATM data and packet data, many ISP operators find that the high acquisition cost and additional maintenance burden of the SONET multiplexer makes its purchase difficult to justify.

In view of the foregoing, there are desired improved devices and methods for facilitating transmission of packet data traffic and ATM data traffic on a single communication link.

SUMMARY OF THE INVENTION

The present invention relates to a combined ATM/packet transmission architecture configured for coupling with a mixed data optical fiber carrying both ATM cells and data packets in a time-division multiplexed manner. The combined ATM/packet transmission architecture includes a transmission convergence device (TCD) circuit having a first TCD input port configured to receive first ATM cells and first data packets from the optical fiber. The TCD circuit has a first TCD output bus configured to output second ATM cells and second data packets from the TCD circuit. The second ATM cells and the second data packets include information from the first ATM cells and the first data packets. The combined ATM/packet transmission architecture includes a combined ATM/packet segmentation-and-reassembly (SAR) circuit having a first SAR input bus configured to be coupled to the first TCD output bus of the TCD circuit to receive the second ATM cells and the second data packets, wherein the combined ATM/packet SAR circuit includes a first SAR output port configured to output first mixed data packets from the combined ATM/packet SAR circuit, the first mixed data packets include information from both the second ATM cells and the second data packets.

The invention relates, in one embodiment, to a processor-based architecture having a processor for facilitating transmission between an ATM port, a first packet port, and a second packet port. The processor-based architecture includes random access memory and a processor coupled to the random access memory and configured to receive ATM cells from the ATM port and first packets from the first packet port and for outputting second packets containing information from both the ATM cells and the first packets on the second packet port. The processor-based architecture includes segmentation-and-reassembly to facilitate bi-directional packet-to-ATM translation functionality. In one embodiment, the processor-based architecture is implemented on a single card.

In another embodiment, the invention relates to a segmentation-and-reassembly engine, which includes a bus interface for receiving both ATM cells and first packets. The segmentation-and-reassembly engine includes first interface logic block for receiving the ATM cells and the first packets from the bus interface and for segregating the ATM cells

from the first packets. The segmentation-and-reassembly engine further includes a second interface logic block coupled to the first interface logic block for receiving the first packets from the first interface logic block to output the first packets. There is further included a reassembly engine coupled to the first interface logic block for receiving the ATM cells and for reassembling the ATM cells into second packets. There is also included a buffer circuit coupled to the reassembly engine and the second interface logic block, the buffer circuit being configured to buffer the second packets for output by the second interface logic block.

These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. 1A illustrates an Internet service provider, representing a location in the current network where SAR engines may be found

FIG. 1B shows an architecture that includes a SONET multiplexer for combining ATM and packets on a fiber.

FIG. 2A shows a prior art ATM transmission architecture that includes a SAR engine and a conventional ATM transmission convergence device (TCD)

FIG. 2B shows a prior art ATM and packet transmission architecture in which ATM cells are received and transmitted via PHY device, and separately packets are received and transmitted via either a 10/100 Ethernet PHY device or a gigabit Ethernet PHY device.

FIG. 3 shows the inventive combined ATM/packet transmission architecture that includes a modified SAR and a combined ATM/packet transmission convergence device to permit both the ATM data traffic and packet data traffic to be merged on a mixed data optical fiber.

FIG. 4 shows in accordance with one embodiment of the present invention the combined ATM/packet TCD of FIG. 3 in greater detail.

FIG. 5 shows, in accordance with one embodiment of the present invention, a receive Utopia & POS-PHY interface.

FIG. 6 shows, in accordance with one embodiment of the present invention, a transmit Utopia & POS-PHY interface.

FIG. 7 shows, in accordance with one embodiment of the present invention, a receive POS-PHY interface.

FIG. 8 shows, in accordance with one embodiment of the present invention, a transmit POS-PHY interface.

FIG. 9 shows, in accordance with one embodiment of the present invention, a processor-based architecture for facilitating integrated data transfer between both ATM and packet traffic with a packet bus or packet link, including bidirectional ATM-to-packet SAR functionality for ATM traffic.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or

all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

In accordance with one aspect of the present invention, there is provided a combined ATM/packet transmission architecture, which receives data packets and transmits the received data packets either as ATM cells or as transmitted data packets on a mixed data optical fiber. On the receive side, the combined ATM/packet transmission architecture receives both ATM cells and data packets on the mixed data optical fiber and resolves them into data packets to be received. Since only a single optical fiber is required for transmitting both ATM and packet data traffic, substantial reduction in costs of implementation and operation, as well as complexity, may be achieved. Likewise, on the receive side, since only a single optical fiber is required for receiving both ATM and packet data traffic, substantial reduction in costs of implementation and operation, as well as complexity, may be achieved.

In accordance with one aspect of the present invention, data to be transmitted on the mixed data optical fiber via the combined ATM/packet transmission architecture is typically received first in the form of data packets. Depending on whether the destination of a received data packet requires the eventual traversal of an ATM network or a packet network, the payload of the received data packet is correspondingly parsed and packaged into either ATM cells or data packets to be transmitted via the mixed data optical link to its destination. On the other hand, data received from the mixed data optical link, which may contain both data packets or ATM data cells, is demultiplexed into packet stream(s) and ATM stream(s). The packet stream(s) are then delineated into data packets to be received while the ATM stream(s) are delineated into ATM cells, which are then reassembled into data packets to be received.

In accordance with one aspect of the present invention, the combined ATM/packet transmission architecture includes two main functional blocks: a combined ATM/packet transmission convergence device (TCD) and a modified segmentation and reassembly (SAR) engine. In one preferred embodiment, both of these main functional blocks (e.g., both the combined ATM/packet TCD and the modified SAR engine) are implemented in a single integrated circuit chip. It is recognized by the inventors herein that this is especially important for high speed applications, e.g., OC-192 and above since at higher speeds, the speed of the system bus on a board may be a limiting factor. In another preferred embodiment, these main functional blocks (e.g., both the combined ATM/packet TCD and the modified SAR engine) are implemented in two separate integrated circuit chips. In yet another preferred embodiment, these main functional blocks (e.g., both the combined ATM/packet TCD and the modified SAR engine) are implemented in a plurality of network processors. The combined ATM/packet TCD interfaces with the mixed data optical fiber to receive the mixed ATM/packet data stream, to demultiplex the mixed ATM/packet data stream into constituent ATM and packet streams for delineation into ATM cells and data packets respectively. The ATM cells and data packets are then passed onto the modified SAR engine wherein the received ATM cells are reassembled into data packets to be multiplexed into the receive POS-PHY (Packet Over Sonet-Physical layer) signal. On the other hand, data packets received from the combined ATM/packet TCD are multiplexed into the receive POS-PHY signal without the need for reassembly. In either case, the data received via the mixed data optical fiber

is converted into data packets and received as such in the receive POS-PHY signal.

On the transmit side, data to be transmitted out on the mixed data optical fiber is received as data packets initially. The modified SAR engine then packages the payload of the received data packet into either ATM cells or data packets to be transmitted depending whether the destination of the received data packet requires the eventual traversal of an ATM network or a packet network. Thereafter, the ATM cells and data packets to be transmitted are forwarded to the combined ATM/packet TCD, which multiplexes them onto the mixed data stream to be transmitted out on the mixed data optical fiber.

To facilitate discussion of the combined ATM/packet transmission architecture, FIG. 2A shows a prior art ATM transmission architecture that includes a SAR engine 202 and a conventional ATM transmission convergence device (TCD) 204. With reference to FIG. 2A, SAR engine 202 may represent, for example, SAR 164 while ATM TCD 204 may be implemented as part of access router 160 (or backbone router 144 if SAR engine 202 represents SAR 170 of FIG. 1A). The function of the prior art ATM transmission architecture of FIG. 2A, which is conventional, is to translate between ATM cells and data packets during the transmission process.

In FIG. 2A, ATM cells are received at ATM TCD 204 from an ATM link 206, which may represent, for example, a SONET, a DS3 link, or the like. The main function of ATM TCD 204 is to extract ATM cells from the transmission medium in the receive direction. In the transmit direction, ATM TCD 204 inserts the ATM cells to be transmitted into the electrical signal of the transmission medium, thereby allowing the transmission of the ATM cells over ATM link 206. ATM TCD 204 is conventional and will not be elaborated further here. SAR engine 202 includes a receive Utopia interface 208, which receives ATM cells from ATM TCD 204 via a Utopia bus 212. Utopia buses are well known to those familiar with the ATM art. The received ATM cells are then passed on to a reassembly engine 214, which reassembles the received ATM cells into packets to be received. Packet memory 216 represents a storage location where assembled packets from various streams are buffered for output. Packet memory 216 may also store partially assembled packets that are awaiting the payloads from yet-to-be-received ATM cells to fill them up. Partially assembled packets exist because most packet protocols specify a payload that is substantially larger than the 48-byte payload of the typical ATM cell, and thus multiple ATM cells are required to fill up the payload of such a packet. A receive packet interface (such as POS-PHY) 218 sends the assembled packets onto internal bus 220, which is internal within the router, to permit the assembled packets to be switched to their designated ports (such as the port that services-Ethernet link 162 in FIG. 1A).

On the transmit side, the received data packets are received from an internal bus 228 at a transmit packet interface 230, which are then forwarded to a segmentation engine 232 wherein the payload of a received data packet is mapped onto one or more ATM cells. The ATM cells are then stored at ATM cell memory 234, which acts as a buffer or a shock absorber for high load periods. A transmit Utopia interface 236 then takes the stored ATM cells and forwards them to ATM TCD 204 via a Utopia bus 240 for eventual transmission on ATM link 206.

As can be seen in FIG. 2A, ATM TCD 204 and SAR engine 202 only interface with the ATM network to service

packets which need to be transmitted out as ATM cells on ATM link 206 or to receive ATM cells from ATM link 206 for conversion to received packets. For the router to interface with the packet network, additional circuitry and another set of optical fibers (for transmitting and receiving packets) is involved. For additional background information, FIG. 2B shows a prior art ATM and packet transmission architecture in which ATM cells are received and transmitted via PHY device 203, and separately packets are received and transmitted via either 10/100 Ethernet PHY 222 or gigabit Ethernet PHY 212.

Referring now to FIG. 3, the combination of the modified SAR 302 and the combined ATM/packet TCD 304 permit both the ATM data traffic and packet data traffic to be merged on a mixed data optical fiber 306. Throughout this discussion, it should be kept in mind that data transmission through optical fibers takes place in a single direction only and typically, two optical fibers are required to transmit and receive data (i.e., one for each direction). On the receive side, the mixed ATM/packet data is received into combined ATM/packet TCD 304, which demultiplexes the received data streams into the constituent ATM and packet streams. The constituent streams are then delineated into ATM cells and packets respectively, which are then transmitted via a modified Utopia bus 310 to modified SAR 302.

At modified SAR 302, the ATM cells and packets are received by a receive combined Utopia & POS-PHY interface 312, which separates the traffic into ATM data traffic and packet traffic. Receive Utopia & POS-PHY interface 312 is discussed further in connection with a FIG. 5 below. The ATM traffic is passed onto a reassembly engine 316 and a packet memory 318 for reassembly into packets and temporary storage in the manner discussed earlier in connection with FIG. 2A. On the other hand, the packet traffic is passed directly to a receive POS-PHY interface 320. As shown in FIG. 3, this POS-PHY interface 320 also receives the reassembled packets from packet memory 318. This POS-PHY interface 320 then sends the packets onto an internal bus 322, which is internal within the router, to permit the packets to be switched to their designated ports (such as the port that services Ethernet link 162 in FIG. 1A). Receive POS-PHY interface 320 is discussed further in connection with a FIG. 7 below.

On the transmit side, data packets are received at a transmit POS-PHY interface 340 via an internal bus 338. Transmit POS-PHY interface 340 then determines whether the data within the received data packet should be transmitted as ATM cells or as data packet(s) to its destination. Transmit POS-PHY interface 340 may make this determination by a variety of techniques. For example, transmit POS-PHY interface 340 may be in communication with a bus master that is coupled to internal bus 338. The bus master may be able to inform transmit POS-PHY interface 340 if the packet received should be transmitted as ATM cells or as data packet(s), and if the packet is to be transmitted as ATM cells, what the header information should be for the ATM cells. Alternatively or additionally, transmit POS-PHY interface 340 may be able to ascertain the destination of the packet from the content of the packets (such as by examining the header of an IP data packet), and use that information to ascertain whether the destination requires a traversal of either an ATM network or a packet network and act accordingly. Other techniques may also be employed. Transmit POS-PHY interface 340 is discussed further in connection with FIG. 8 below.

Packets destined for transmission as ATM cells are passed onto a segmentation engine 342 where they will be seg-

mented and mapped onto one or more ATM cells. The ATM cells are then buffered at ATM cell memory 344 for transmission to combined ATM/packet TCD 304 via a transmit Utopia & POS-PHY interface 350 and a modified Utopia bus 352. On the other hand, packet traffic is passed from transmit POS-PHY interface 340 onto transmit Utopia & POS-PHY interface 350 for transmission to combined ATM/packet TCD 304 via modified Utopia bus 352. In combined ATM/packet TCD 304, the ATM cells and packets are multiplexed onto the electrical signal of the transmission standard on mixed data optical fiber 306 (e.g., DS3, OC48, OC192, etc.) for transmission out on the mixed data optical fiber.

FIG. 4 shows in accordance with one embodiment of the present invention combined ATM/packet TCD 304 of FIG. 3 in greater detail. On the receive side, the mixed ATM and packet data streams are received initially by a receive framer 402, which frames up the electrical signal to ascertain where the data resides in the electrical signal. Thereafter, a TDM demultiplexer 404 demultiplexes the received mixed data streams into ATM streams and packet streams in accordance with a time division demultiplex scheme. The ATM data streams are received by a cell delineation circuit 408, which finds out the beginning and end of the cells, obtain the cells, and perform any error checking such as CRC error checking. The packet data streams are received by a packet delineation circuit 410, which also delineates packets, obtain the packets, and perform any error checking such as CRC error checking. The ATM cells and data packets are then temporarily stored in a ATM cell memory 412 and a packet memory 414 respectively.

Thereafter, the ATM cells and data packets are output by receive Utopia & POS-PHY interface 416 via modified Utopia bus 310 (also shown in FIG. 3) to be received by receive Utopia & POS-PHY interface 312 of FIG. 3. Receive Utopia & POS-PHY interface 416 is discussed further in connection with FIG. 6 below. Preferably associated with each ATM cell or data packet transmitted from receive Utopia & POS-PHY interface 416 (of FIG. 4) to receive Utopia & POS-PHY interface 312 (of FIG. 3) is a signal which indicates whether the data received by receive Utopia & POS-PHY interface 312 is an ATM cell or a data packet to permit receive Utopia & POS-PHY interface 312 to handle the data appropriately (i.e., to perform reassembly or to pass directly to receive Utopia & POS-PHY interface 320 of FIG. 3).

On the transmit side, the ATM cells and data packets received from transmit Utopia & POS-PHY interface 350 of FIG. 3 are received by transmit Utopia & POS-PHY interface 450 of FIG. 4. Transmit Utopia & POS-PHY interface 450 is discussed further in connection with FIG. 5 below. Transmit Utopia & POS-PHY interface 450 ascertains whether the received data is ATM or packet and passes the ATM cells to an ATM cell memory 452, and the packets to a packet memory 454. Thereafter, a cell assembler 456 performs insertion of the ATM cells from ATM cell memory 452 into the TDM stream while a packet assembler 458 likewise performs insertion of the packets from packet memory 454 into the TDM stream. If there is no active cell or packet, an idle cell or packet may be inserted. A TDM multiplexer 460 multiplexes the ATM stream from cell assembler 456 and the packet stream from packet assembler 458 into a single stream on bus 462, which is then mapped by a transmit framer 464 into the electrical signal of the mixed data optical fiber 306 for transmission onward.

FIG. 5 shows, in accordance with one embodiment of the present invention, a receive Utopia & POS-PHY interface 502, representing one suitable for use in block 312 of FIG.

3 or block **450** of FIG. 4. With reference to FIG. 5, both ATM cells and packets are received at a terminate receive Utopia & POS-PHY signal circuit **504**. The ATM cells and packets may be received from, for example, the combined ATM/packet TCD **304** of FIG. 3 via the modified Utopia bus **320**.

Terminate receive Utopia & POS-PHY signal circuit **504** acts to terminate the electrical signals as part of the Utopia standard. However, the modified Utopia bus preferably includes an additional signal that indicates whether the data received is an ATM cell or a data packet. This information is obtained by, for example, receive Utopia & POS-PHY interface circuit **416** within combined ATM/packet TCD **304** when it receives either an ATM cell or a data packet from ATM cell memory **412** or packet memory **414**.

After termination, this information along with the received data is passed on to circuit block **506**, which determines whether an ATM cell or a data packet is received and send the ATM cell or data packet to its respective forwarding circuits **508** or **510**. In the case of an ATM cell, forward circuit **508** then forwards the ATM cell to, for example, reassembly engine **316**. On the other hand, in the case of a data packet, forward circuit **510** then forwards the data packet to, for example, receive POS-PHY interface **320** for eventual forwarding via internal bus **322**.

FIG. 6 shows, in accordance with one embodiment of the present invention, a transmit Utopia & POS-PHY interface **602**, representing one suitable for use in block **350** of FIG. **3** or block **416** of FIG. **4**. With reference to FIG. **6**, ATM cells and packets are received at ATM storage circuit **604** and packet storage circuit **606**. The packets and ATM cells may be received from, for example, the transmit POS-PHY interface **340** or from ATM cell memory **344**. Thereafter, a transmit gating circuit **608** then decides whether an ATM cell or a packet should be output. The decision may be made based on, for example, information received from combined ATM/packet TCD **304**, which provides information about whether ATM cell memory **452** or packet memory **454** is ready to accept another ATM cell or packet respectively. By way of example, both of whether ATM cell memory **452** or packet memory **454** may be polled and two signals may be furnished via the modified Utopia interface **352** from combined ATM/packet TCD **304** to furnish the desired information to transmit gating circuit **608** of transmit Utopia POS-PHY interface **350**. Terminate transmit Utopia & POS-PHY signal circuit **504** acts to terminate the electrical signals substantially in accordance with the Utopia standard with modified Utopia bus **612** as shown.

FIG. 7 shows, in accordance with one, a receive POS-PHY interface **702**, representing one suitable for use in block **320** of FIG. **3**. With reference to FIG. **7**, packets reassembled from ATM cells and packets that are received as packets and does not need translation are received into storage circuit **704** and storage circuit **706** respectively as shown. These packets may be received from, for example, from packet memory **318** or the receive Utopia & POS-PHY interface **312**. Thereafter, a multiplexing circuit **708** multiplexes the received ATM cells and packets into a single stream to be transmitted out to the internal bus **712** (such as internal bus **322** of FIG. **3**). Multiplexing may be done in accordance with, for example, a time-division multiplex scheme. Terminate receive POS-PHY signal circuit **710** acts to terminate the electrical signals substantially in accordance with the POS-PHY standard scheme for transmission.

FIG. 8 shows, in accordance with one, a transmit POS-PHY interface **802**, representing one suitable for use in block **340** of FIG. **3**. With reference to FIG. **8**, the packets are

received from the internal bus **804** into a termination circuit **804**, which terminates the electrical signals as part of the POS-PHY standard scheme. Thereafter, the packets received into demultiplexing circuit **806**, which demultiplexes the packets into streams destined for the ATM network or the packet network. Demultiplexing may be performed using any number of demultiplexing techniques, including those discussed earlier in connection with block **340** of FIG. **3**.

After demultiplexing, packets destined for the ATM network are forwarded to a buffer block **808** for transmission to the segmentation engine (e.g., segmentation engine **342** of FIG. **3**). Once segmented into ATM cells, the ATM cells are then forwarded to a transmit Utopia & POS-PHY interface (such as transmit Utopia & POS-PHY interface **350** of FIG. **3**) for eventual transmission to the combined ATM/packet TCD. On the other hand, packets destined for the packet network are forwarded to a buffer block **810** for transmission to a transmit Utopia & POS-PHY interface (such as transmit Utopia & POS-PHY interface **350** of FIG. **3**) for eventual transmission to the combined ATM/packet TCD.

Table 1 below shows the signals associated with one embodiment of the modified Utopia bus.

TABLE 1

Signals for modified Utopia Interface			
Utopia	POS-PHY	Modified Utopia	Description
TxClock	TxClock	POS/ATM	Mode selection
TxAddr	TxAddr	TxClock	Transmit Clock
TxData	TxData	TxAddr	Transmit Address
	TxMod	TxData	Transmit Data
	TxSOC	TxBgn	Byte Enables
	TxEOP	TxEnd	Transmit Start of Cell/Packet
TxPry	TxPry	TxPry	Transmit End of Cell/Packet
TxEnb	TxEnb	TxEnb	Transmit Parity
TxErr	TxErr	TxErr	Transmit Select/Enable
TxCA	TxCA	TxCA	Transmit Error
	TxPA	TxPA	Transmit Cell Available
RxClock	RxClock	RxClock	Transmit Packet Available
RxAddr	RxAddr	RxAddr	Receive Clock
RxData	RxData	RxData	Receive Address
	RxMod	RxMod	Receive Data
	RxVal	RxVal	Byte Enables
RxSOC	RxSOC	RxBgn	Receive Start of Cell/Packet
	RxEOP	RxEnd	Receive End of Cell/Packet
RxPry	RxPry	RxPry	Receive Parity
RxEnb	RxEnb	RxEnb	Receive Select/Enable
RxErr	RxErr	RxErr	Receive Error
RxCA	RxCA	RxCA	Receive Cell Available
	RxPA	RxPA	Receive Packet Available

As can be appreciated from the foregoing, the inventive combined ATM/packet transmission architecture permits both ATM traffic and packet traffic to be sent over a single optical fiber and received over another single optical fiber. This is advantageous in view of technologies that broaden the bandwidth of existing optical fibers such as DWDM (dense wave division multiplex).

Furthermore, it is expected that the volume of data carried by packet-centric networks will change over time relative to the amount of data carried by ATM networks. For network operators, the inventive combined ATM/packet transmission architecture furnishes a seamless migration path as the relative volume of data traffic between the two networks changes. By way of example, as customers migrate toward packet-oriented networking equipment over time, the volume of packet-oriented traffic may increase relative to the volume of ATM traffic may increase over time. In this case,

the receive and the transmit Framers in the combined ATM/packet TCD may be appropriately configured to handle different traffic load mixes over the mixed data optical fiber.

Still further, the receive and the transmit Framers may be appropriately configured to provision the mixed data optical fiber such that only a portion of the maximum bandwidth is employed for data transmission. In a tariff-based regime wherein operators may be required to pay for different classes of traffic, different types of traffic (e.g., ATM vs. packet vs. SONET), and/or the actual bandwidth employed or reserved, such flexible provisioning capability may be highly advantageous and/or desired by network operators. This is done by setting software registers which allocate each TDM slot to either ATM or packet traffic.

In a preferred embodiment, the modified SAR is implemented as a single chip in order to handle high speed optical data received and/or transmitted via the optical fibers. Although the single chip implementation may seem less flexible than a network processor approach and requires extensive engineering on a single die, the single chip implementation is particularly advantageous since at high speeds, a multi-ICs approach for combining ATM and packet data can become almost impossible to implement because the backplane of a board containing the multiple ICs becomes a speed bottleneck. It is also preferred that the inventive architecture for combining ATM/data packets be implemented into a router (such as a backbone router) so that the router can now perform the function of aggregating both data packets and ATM cells. With reference to FIG. 1, the modified SAR can be implemented in place of SAR 170, and a single optical fiber coupled thereto can serve to transmit both ATM cells to the ATM backbone and data packets to the POS backbone, and another single optical fiber coupled thereto can serve to receive both ATM cells from the ATM backbone and data packets from the POS backbone.

The inventive combined ATM/packet transmission architecture also renders it unnecessary to purchase and maintain a SONET multiplexer system, which is typically a complex and expensive piece of equipment, when operators wish to combine ATM traffic and packet traffic on a single optical fiber. Besides eliminating the SONET multiplexer acquisition cost, the inventive ATM/packet transmission architecture also reduces the number of system boxes that an ISP has to maintain and upgrade, thereby leading to reduced operation cost.

In another aspect of the invention, network operators may desire the high degree of software-programmable flexibility and control over the feature set that a processor approach offers. Accordingly, a processor-based architecture (e.g., either a network processor card or any processor implemented as a processor card, a server, or the like) may be employed to perform the function of receiving both ATM cells and packet data and perform the SAR function, and more specifically the reassembly function, to convert the ATM cells to packets for transmission out along with the received packets on a link or a bus. In the reverse direction, the processor-based architecture is employed to perform the function of receiving packets destined for transmission out as ATM cells or as packets. The processor-based architecture may distinguish between the two using a technique similar to that discussed in connection with FIG. 3 or using any suitable discrimination criteria or technique. The processor-based architecture then performs the SAR function on the packets containing data destined for transmission as ATM cells, or more specifically the segmentation function, to convert these packets to ATM cells. The ATM cells and the

received packets destined for transmission out as packets are then transmitted onward.

More preferably, one aspect of the invention relates to using a single card, backplane, or system having therein a processor, memory, and associated logic to receive both ATM cells and packet data, performing the SAR function on the ATM cells, and outputs the packets or resolving the received packets into ATM cells and packets to be transmitted to their respective links in the reverse direction. This is shown in FIG. 9 wherein the processor-based architecture 902 (implemented as a single card in this example as evidenced by card connector 930) having therein a processor 904 and associated memory and logic (not shown to improve clarity) is employed to perform the reassembly function on the ATM cells input at port 906 and the segmentation function on the packets received at port 908 but destined for transmission out as ATM cells on ATM port 906. However, as shown in FIG. 9, the processor-based architecture also handles, in an integrated manner, packets passed between port 908 and port 910. Although each of these ports is shown to be bi-directional, it should be understood that the port may represent an optical port coupled to an optical fiber infrastructure, which typically passes information in only one direction per fiber (in which case, a pair of fibers is employed per port).

More importantly, within the single card or backplane, the relative bandwidth of ATM/packet may be dynamically adjusted by software control, e.g., to account for different traffic condition and/or to provide a migration path toward the packet centric network in the manner discussed earlier. Although the network processor-based architecture may not be as suitable for extremely high speed operation (e.g., OC-768 based on today's processor speed), it offers programmable flexibility, and the ability to integrate both ATM cells and packets SAR function in a single card or single backplane offers advantages to network operators who have to deal with limited space and/or limited card slots and/or dynamically changing traffic condition and/or need to have control over the full feature set in a more tightly integrated way. This is unlike the prior art approach wherein the SAR function is implemented on a card that only receives ATM traffic, and another card must be required to accept packet traffic and there is little, if any, ability to dynamically adjust the relative bandwidth between the two.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents, which fall within the scope of this invention. By way of example, although data packets out of the SAR is outputted in the packet-over-SONET format, they may also be outputted as packet-over-DWDM. As another example, although a single processor is shown in the example employed to discuss the processor-based architecture, it should be noted that the use of multiple or parallel processors (which technique is well developed in the computing art) is also within the scope of the present invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

1. A segmentation-and-reassembly engine, comprising:
a bus interface for receiving a combined input stream having ATM cells formatted as ATM cells and first packets formatted as packets;
a first interface logic block for receiving said ATM cells and said first packets from said bus interface and for segregating said ATM cells from said first packets;

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a second interface logic block coupled to said first interface logic block for receiving said first packets from said first interface logic block to output said first packets;

a reassembly engine coupled to said first interface logic block for receiving said ATM cells and for reassembling said ATM cells into second packets; and

a buffer circuit coupled to said reassembly engine and said second interface logic block, said buffer circuit being configured to provide first and second packets for output in a combined output stream having first and second packets formatted as packets.

2. A segmentation-and-reassembly engine as recited in claim 1, wherein said segmentation-and-reassembly engine is provided on a single integrated circuit chip.

3. An apparatus for processing data, said apparatus comprising:

a first interface logic block for receiving a combined input stream having ATM cells formatted as cells and first packets formatted as packets and for segregating said ATM cells from said first packets;

a second interface logic block coupled to said first interface logic block for receiving said first packets from said first interface logic block to output said first packets;

a reassembly engine coupled to said first interface logic block for receiving said ATM cells and for reassembling said ATM cells into second packets; and

a buffer circuit coupled to said reassembly engine and said second interface logic block, said buffer circuit configured to provide first packets and second packets for output in a combined output stream having first and second packets formatted as packets.

4. An apparatus as recited in claim 3, wherein said apparatus further comprises:

a combine ATM/packet transmission convergence device coupled to said first interface logic block to supply said ATM cells and said first packets, said combined ATM/packet transmission convergence device receives a mixed data stream and converts the mixed data stream into said ATM data and said packet data.

5. An apparatus as recited in claim 4, wherein said combined ATM/packet transmission convergence device further supplies a data type signal to said bus interface so that said bus interface can distinguish said ATM data from said packet data.

6. An apparatus as recited in claim 5, wherein said apparatus is provided on a single integrated circuit chip.

7. An apparatus for processing ATM data and packet data, said apparatus comprising:

an input interface that receives incoming data in a combined input stream including both ATM cells formatted as ATM cells and packets formatted as packets and separates the incoming data into at least incoming ATM data and incoming packet data;

a reassembly engine operatively connected to said input interface, said reassembly engine operates to receive the incoming ATM data from said input interface and reassemble the incoming ATM data into reassembled packet data; and

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an output interface operatively connected to said input interface and said reassembly engine, said output interface configured to output data formatted as packets in a combined output stream.

8. An apparatus as recited in claim 7, wherein said output interface comprises a multiplexer, said multiplexer operates to multiplex the incoming packet data and said reassembled packet data into a single output data stream.

9. An apparatus as recited in claim 8,

wherein said input interface receives a control signal, and wherein said input interface determines whether the incoming data is the incoming ATM data or incoming packet data based on the control signal.

10. An apparatus as recited in claim 9, wherein the incoming data and the control signal are received at said input interface via a modified Utopia bus.

11. A method for transmitting ATM data and packet data over a shared transmission medium, said method comprising:

receiving a combined input data stream having ATM cells formatted as ATM cells and first packets formatted as packets;

separating the incoming data stream into at least incoming ATM data and incoming packet data;

reassembling the incoming ATM data into reassembled packet data; and

thereafter transmitting the incoming packet data and the reassembled packet data in packet format over the shared transmission medium in a combined output stream.

12. A method as recited in claim 11, wherein said transmitting comprises:

multiplexing the incoming packet data and the reassembled packet data over the shared transmission medium.

13. A method as recited in claim 12, wherein the incoming ATM data and the incoming packet data are transmitted over the shared transmission medium as packet data.

14. A method as recited in claim 11, wherein the transmission medium is an optical fiber.

15. A method as recited in claim 11, wherein said separating comprises:

examining the incoming data to obtain a data type indication; and

segregating the incoming ATM data and incoming packet data based on the data type indication.

16. A method as recited in claim 15, wherein the data type signal is an additional signal within the incoming data.

17. A method as recited in claim 15, wherein the transmission medium is an optical fiber.

18. A method as recited in claim 15, wherein said transmitting comprises:

multiplexing the incoming packet data and the reassembled packet data over the shared transmission medium.

19. A method as recited in claim 11, wherein said method is performed by an integrated circuit chip.

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